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(71) Applicant: QUALCOMM INCORPORATED [US/US]; 5775 Morehouse Drive, San Diego, CA 92121-1714 (US).

(72) Inventors: AGRAWAL, Avneesh; 655 South Fair Oaks #109, Sunnyvale, CA 94086 (US). BENDER, Paul, E.; 2879 Angell Avenue, San Diego, CA 92122 (US). BUTLER, Brian, K.; 8736 Glenwick Lane, La Jolla, CA 92037 (US). HANSQUINE, David, W.; 7510 Charmant Drive, San Diego, CA 92122 (US).

(74) Agents: MILLER, Russell, B. et al.; Qualcomm Incorporated, 5775 Morehouse Drive, San Diego, CA 92121-1714 (US).

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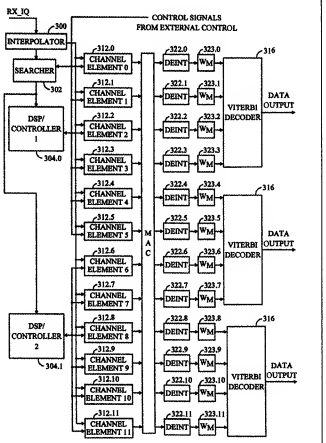
(57) Abstract

A wireless communications system is described. In one embodiment of the invention, a set of demodulation resources demodulates a set of signals that can transmit data at a set of rates. For signals transmitting at lower data rates, a single demodulation resource demodulates an entire signal. For signals transmitting at higher data rates, two or more demodulation resources each demodulate a portion of the signal. Advantageously, the first portion of the higher rate signal is substantially different than the second portion.



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PROCESSING SIGNALS OF DIFFERENT DATA RATES

BACKGROUND OF THE INVENTION

I. Field of the Invention

The present invention is directed to wireless communications. More particularly, the present invention is directed to transmitted data at various rates within a wireless communications system.

II. Description of the Related Art

Mobile digital wireless communications have primarily been used to conduct voice communications. With the advent of the World Wide Web, e-mail and computer networking, the need for data based wireless communications has increased exponentially.

Data communications typically require higher data rates, and a greater variety of data rates, than voice based wireless communications. This increased variety of communication rates typically increases the complexity or circuit size of the systems used to process and generate the transmitted data. Increased complexity, or circuit size, typically increases cost.

The present invention is directed to decreasing complexity and size, and therefore the cost, of systems that process data at a variety of rates.

SUMMARY OF THE INVENTION

A wireless communications system is described. In one embodiment of the invention, a set of demodulation resources demodulates a set of signals that can transmit data at a set of rates. For signals transmitting at lower data rates, a single demodulation resource demodulates an entire signal. For signals transmitting at higher data rates, two or more demodulation resources each demodulate a portion of the signal. Advantageously, the first portion of the higher rate signal is substantially different than the second portion.

BRIEF DESCRIPTION OF THE DRAWINGS

The features, objects, and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout and wherein:

Fig. 1 is a block diagram of a wireless communications system configured in accordance with one embodiment of the invention.

Fig. 2 shows a block diagram of a reverse link transmit system configured in accordance with one embodiment of the invention.

Fig. 3A illustrates the data frame structure for medium rate data transmission used in one embodiment of the invention.

Fig. 3B illustrates the frame format used in one embodiment of the invention for other lower rate frames.

Fig. 4 is a block diagram of a base station configured in accordance with one embodiment of the invention.

Fig. 5 is a block diagram of the demodulation portion of CSM **366** when configured in accordance with one embodiment of the invention.

Fig. 6 is a block diagram of a channel element **312** when configured in accordance with one embodiment of the invention.

Fig. 7 is a block diagram of a finger processor **370** when configured in accordance with one embodiment of the invention. and

Fig. 8 is a block diagram of deinterleaver-demod **322** (**Fig. 5**) when configured in accordance with one embodiment of the invention.

Fig. 9 (2-13) is a block diagram of repetition decovering and symbol drop circuit **516** when configured in accordance with one embodiment of the invention.

Fig. 10 is a block diagram of the symbol drop block when configured in accordance with one embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A wireless communications system is described. The exemplary embodiment is described in the context of the reverse link of a cellular telephone system. While use within this context is advantageous, different embodiments of the invention may be incorporated in different environments or configurations. In general, the various systems described

herein may be formed using software controlled processors, integrated circuits or discreet logic. More exotic implementations are also consistent with the use of the present invention including the use of biological or chemical computational systems.

Additionally, the data, instructions, commands, information, signals, symbols and chips that may be referenced throughout the application are advantageously represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or a combination thereof. In addition, the blocks shown in each block diagram may represent hardware or method steps.

Fig. 1 is a block diagram of a wireless communications system configured in accordance with one embodiment of the invention. Subscriber units **10a** and **10b** interface with base station **14** using digitally modulated radio frequency signals. The reverse link is the signal transmitted from subscriber units **10a** and **10b** to base station **14**, and the forward link is the signal transmitted from base station **14** to subscriber units **10**. Base station controller (BSC) **16** and mobile switching center (MSC) **18** provide call and data routing functionality as well as call mobility management.

Both the reverse link and the forward link transmit various types of data at various rates. For example, voice based telephone calls are conducted using data rates on the order of ten (10) kilobits per second (Kbits/sec). Data rates on the order of 64 Kbits/sec are used to conduct data communications for applications such as web browsing, and video conferencing. Illustratively, subscriber unit **10a** is shown as a cellular telephone and subscriber unit **10b** is shown as a laptop computer.

Fig. 2 shows a block diagram of a reverse link transmit system configured in accordance with one embodiment of the invention. As illustrated by **Fig. 1**, a system typically includes multiple transmit systems **10** like that shown in **Fig. 2** (shown as a cellular telephone and computer) transmitting to a base station **14** at any given time. In one embodiment of the invention, some of the subscriber units **10** may be transmitting to base station **14** in accordance techniques other than that shown in **Fig. 2**. For example, some subscriber units **10** may transmit in accordance with the IS-95 standard, or one of its derivatives, while other subscriber units **10** transmit in accordance with that shown in **Fig. 2**. A system and method for processing RF signals substantially in accordance with the use of the IS-95 standard is described in US patent 5,103,459 entitled "System and Method for Generating Signal Waveforms in a CDMA Cellular Telephone System" assigned to the

assignee of the present invention and incorporated herein by reference ('459 patent).

Still referring to **Fig. 2**, during "low data rate mode" data frames are received on input A1, with each data frame containing one of four possible amounts of data. The different amounts of data correspond to different data rates, with a set of different data rates referred to as a "rate set." Lower data rate mode typically corresponds to voice based communication, with the four data rates corresponding to four different amount of voice activity. CRC generator **100.1** adds CRC checksum bits to some of the frames depending on the rate and rate set. Additionally, tail bits of known value (preferably all logic zero) are added by tail bit generator **102.1** to each frame. The number of tail bits is preferably equal to k-1, where k is the depth of the coder. In one embodiment of the invention eight tail bits are added.

In one embodiment of the invention, two different rate sets are available. The different rate sets correspond to two different levels of voice quality, with the rate set having the highest data rates being the one with the highest voice quality. The different rate sets are differentiated by the highest rate (or "rate one") within each set, which is 9.6 Kbits/sec for a first rate set (8K Rate set) and 14.4 Kbits/sec for a second rate set (13K Rate set). The three (3) additional rates within a rate set are referred to as half (1/2) rate, quarter (1/4) rate, and eighth (1/8) rate, based on the approximate fraction of that rate in comparison with rate one. Such lower data rates are similar to those found is the IS-95 and IS-95B wireless telecommunications over-the-air interface standards.

To conduct "medium" rate transmissions (i.e. a transmission at a higher rate than those available in low data rate mode) using the system shown in **Fig. 2**, additional data is input at inputs A2 - A8. In one embodiment of the invention, the total number of inputs A1 - A8 used must be an integer power of two. This provides medium rates transmissions approximately equal to two (2) times (rate two), four (4) times (rate four) and eight (8) times (rate eight) the rate one rate of either of the two rate sets (8K and 13K).

This modulation provides six 6 additional medium transmission rates, and a total of fourteen possible rates overall. The fourteen rates can be divided into two sets: one associated with the 13K, and the other associated with the 8K. Together the fourteen data rates are rate eight, rate four, rate two, rate one, half rate, quarter rate and eighth rate for 8K, and rate eight, rate four, rate two, rate one, half rate, quarter rate and eighth rate for 13K. In one embodiment of the invention, a subscriber unit **10** operates in either

lower data rate mode or medium data rate mode. However in other embodiments of the invention, a subscriber unit may operation at any available data rate.

The data received on inputs **A1 -A8** during "medium data rate mode" is time multiplexed by multiplexer **104** into a single data stream that is convolutionally encoded by covolutional encoder **106** at a rate dependent on the data rate as described below. Repeater **108** performs symbol repetition for rate one or lower transmission rates at a rate R (rate one through eighth rate, referred to herein as "lower rates") for either 8K or 13K rate sets, and Walsh cover modulates the lower rate transmissions with a low rate Walsh code W_L that is also dependent on the data rate.

Puncture circuit **110** punctures the data stream for data transmissions associated with 13K frames by a puncture factor P. A puncture factor P of 1/3 means that one of every three code symbols is removed from the data stream. This effectively reduces the coding rate performed on the data, but allows more data to be transmitted thereby increasing the data rate. For example, if encoder **106** performs R=1/4 encoding, and the puncture factor P is 1/3, the effective coding rate $R_E = 3/8$.

Interleaver **112** performs block interleaving on 20 ms blocks of the data being transmitted, whatever the data rate. Thus, the amount of data, or the number of code symbols, interleaved at any given time is dependent on the data transmission rate.

Medium rate repeat circuit **114** performs medium rate repeating according to a medium rate repeat factor R_M. Additionally, for medium rate data transmissions (rates two, four and eight), medium rate Walsh cover circuit **116** modulates the symbols with a medium rate Walsh code W_M that is dependent on the higher data rate being used.

The various parameters used for the system of **Fig. 2** in one embodiment of the invention are set forth in Table I.

	R_L	R_M	Coding Rate	P	Low Rate Walsh Code W_L	Medium Rate Walsh Code W_m
Eighth $Rate_8$ (1/8)	16	8	1/4		++++++++ - - - - - - - -	
Quarter $Rate_8$ (1/4)	8	8	1/4		++++ - - - -	
Half $Rate_8$ (1/2)	4	8	1/4		++ - -	
Rate One_8 (1)	2	8	1/4		+ -	
Eighth $Rate_{13}$ (1/8)	16	8	1/4	1/3	++++++++ - - - - - - - -	
Quarter $Rate_{13}$ (1/4)	8	8	1/4	1/3	++++ - - - -	
Half $Rate_{13}$ (1/2)	4	8	1/4	1/3	++ - -	
Rate One_{13} (1)	2	8	1/4	1/3	+ -	
Rate Two_8	1	4	1/4			++++ - - - -
Rate $Four_8$	1	2	1/4			++ - -
Rate $Eight_8$	1	1	1/4			+ -
Rate Two_{13}	1	4	1/4	1/3		++++ - - - -
Rate $Four_{13}$	1	2	1/4	1/3		++ - -
Rate $Eight_{13}$	1	1	1/4	1/3		+ -

Table I.

Where a Walsh code entry is left blank, no Walsh code modulation is performed. The subscript for each rate (8 or 13) indicates whether the particular data rate is associated with the 8K or 13K rate. As should be apparent, the repeat rate R_L and R_M are adjusted so that the effective symbol rate remains constant. Keeping the effective symbol rate constant simplifies processing of the variable rate data both at the transmit and receive ends. Performing low and medium rate Walsh code modulation at different stages in the processing facilitates differentiating low rate transmission from medium rate transmissions. For both low and medium data rates, the Walsh code modulation further facilitates determining the rate at which the data is being sent.

In one embodiment of the invention, gating circuit **118** performs gating for eighth rate frames in order to conserve power. This gating comprises transmitting only the last half, or 10 ms, of the frame. Additionally, gating circuit **118** may, when the subscriber unit **10** is in a "search mode," gate half rate and quarter rate frames as well. The gating for these frames is preferably performed like that for the eighth rate frames. That is, the first half, or 10 ms, of the frame is blocked. During the gating of any of the frames, the subscriber unit **10** can search for other forward link signals at frequency bands not currently being processed. This facilitates performing hard handoff, which occurs when the subscriber unit switches the frequency band at which it operates (as well as in other instances).

The resulting chip stream from gating circuit **118** is repeated by 2x circuit **120** and the output of 2x circuit **120** is covered by the Walsh traffic channel code Wc,t using an XOR gate **122** and then gain adjusted by traffic channel gain adjust Gt using multiplier or amplifier **124**. Additionally, pilot data is multiplexed with control data, repeated by 2x circuit **120**, and covered with a control channel Walsh code Wc,c using an XOR gate **122**. The pilot channel may also be gain adjusted in some embodiments of the invention.

The control data is typically power control commands, which are generated in response to the forward link signal, and indicate whether the transmit power of the channel in the forward link signal allocated for communicating with the terminal should be increased, decreased or held steady.

The resulting traffic channel data and control channel data are complex multiplied with an in-phase PN code and a quadrature phase PN code using complex multiplier **126**, yielding an in-phase term X_I and a quadrature phase term X_Q. The inphase term X_I and the quadrature phase term X_Q are filtered by low pass filters **128**, upconverted with an in-phase

carrier and a quadrature-phase carrier respectively using mixers **130**, summed by summer **132**, gain adjusted by amplifier **134**, and then transmitted.

Fig. 3A illustrates the data frame structure for medium rate data transmission used in one embodiment of the invention. As noted above, in one embodiment of the invention, each frame corresponds to a 20 ms duration.

For rate one frames **150**, the frame is comprised of data field **160**, a CRC checksum field **162**, and a tail data field **164**. The tail data field **164** is used during encoding to clear the convolutional coder and assists in decoding. The tail data field **160** can be any known data sequence. To fully clear the decoder, the length of the data sequence is one less than the convolution coding depth K. In one embodiment of the invention, the coding depth K is nine (9) and the tail data filed **164** is comprised of eight (8) logic zeros. While the use of a CRC checksum field **162** and a tail data field **164** are preferred, other embodiments of the invention may use different "control" fields.

For rate two frame **152**, the frame is comprised of data fields **160.2** and **160.3**, CRC fields **162.2** and **162.3** and tail data fields **164.2** and **164.3.** In one embodiment of the invention, the format and size of data fields **160.2** and **160.3** corresponds to data field **160.1**. Similarly, the format and size of CRC fields **162.2** and **162.3** are the same as that of CRC field **162.1** and the format and size of tail data fields **164.2** and **164.3** are the same as tail data field **164.1**.

For rate four frame **152**, the frame is comprised of data fields **160.4**, **160.5**, **160.6** and **160.7**, CRC fields **162.4**, **162.5**, **162.6** and **162.7** and tail data fields **164.4**, **164.5**, **164.6**, and **164.7.** In one embodiment of the invention, the format and size of data fields data fields **160.4**, **160.5**, **160.6** and **160.7** corresponds to data field **160.1** (and therefore to of data fields **160.2** and **160.3**). Similarly, the format and size of CRC fields **162.4**, **162.5**, **162.6** and **162.7** are the same as that of CRC field **162.1** and the format and size of **164.4**, **164.5**, **164.6**, and **164.7** are the same as tail data field **164.1**.

For rate eight frames, the frame is comprised of data fields **160.8 - 160.15**, CRC fields **162.8 - 162.15** and tail data fields **164.8 - 164.15.** In one embodiment of the invention, the format and size of data fields data fields **160.8 - 160.15** corresponds to data field **160.1** (and therefore to of data fields **160.2** and **160.7**). Similarly, the format and size of CRC fields **162.8 - 162.15** are the same as that of CRC field **162.1** and the format and size of **164.8 - 164.15** are the same as tail data field **164.1**.

Having the format and size of the various fields be the same as the corresponding fields in different rate frames facilitates processing of the different rate frames. In particular, circuitry used to generate frames of one rate may be used to generate higher rate frames simply by increasing the rate at which those circuits operate. Allowing the same circuitry to be used for the different rate frames reduces the total amount of circuitry necessary to perform the necessary transmit and receive processing, and therefore reduces the size and cost of any integrated circuit or system operating in accordance with some embodiments of the inventions. Also, the rate of processing is increased because fewer alterations to the processing path are necessary.

Increasing the rate of operation of a circuit can take many forms including reducing the time sharing of the circuit or increasing the duration of operation of the circuit during each frame. Also, while a preferred embodiment of the invention has the corresponding fields of different rate frames the same in both format and size to maximize circuitry reuse, other embodiments of the invention may only have some attributes of the corresponding fields the same or similar.

For example, the size of the corresponding fields may be the same, but not the format. Or, the format can be the same for a portion of the data for some fields, but different rate frames may have additional data in those fields. In other embodiments, the field size and formats may be different, but the order of the fields repeats in the same order with respect to order of other rate frames. In each case, similarities between the fields, size, formatting or both, of the various rate frames facilitates both receive and transmit processing of the data.

In one embodiment of the invention, for data frame processed substantially in accordance with the IS-95 standard, the data field size decreases as the transmission rate decreases, and the number of bits transmitted is decreased by transmit gating. A system and method for formatting lower rate frames is described in US Patent 5,504,773 entitled "METHOD AND APPARATUS FOR THE FORMATING OF DATA FOR TRANSMISSION" assigned to the assignee of the present invention and incorporated herein by reference.

For other lower rate frames, such as some of those listed in Table I, the frame format used in one embodiment of the invention is shown in **Fig. 3B**. Each frame is comprised of user data **170**, CRC data **172** and tail bit data **174**. The number of bits of some type of data varies from rate to rate as shown.

For the high data rates, the rate one frame format is used for each set of user, CRC, and tail data field in one embodiment of the invention.

Fig. 4 is a block diagram of a base station configured in accordance with one embodiment of the invention. RF units **362** receive RF signals via the antennas, and filter, downconvert and digitize the RF signals generating baseband samples. In one embodiment of the invention, each antenna and RF unit are used to provide telephone service to a sector of the coverage area of the base station. Each sector typically has more than one antenna as well for additional diversity.

The baseband samples are received by cell cite modem (CSM) **366** which is controlled by control unit **364**. CSM is typically an integrated circuit. Control unit **364** is typically a microprocessor controlled by software instructions stored in memory in one embodiment of the invention. CSM **366** demodulates a set of signals contained in the baseband receive samples generating data that is forwarded to data formatter **368**. Data formatter **368** places the data in packets containing address information and forwards the packets to a base station controller.

In other embodiments of the invention, separate systems or integrated circuits perform the modulation and demodulation functions performed by CSM **366**.

Fig. 5 is a block diagram of the demodulation portion of CSM **366** when configured in accordance with one embodiment of the invention. During typical operation of the exemplary embodiment of the invention provided herein, the signal processing circuit receives and processes reverse link signals generated by transmit systems like that shown in **Fig. 2**. The circuit is preferably implemented on a single integrated circuit, with the control functionality provided either on the same integrated circuit or externally. The control functionality is typically performed by a microprocessor running software stored in memory. In general, tasks are divided between the microprocessor and the DSPs as described herein; however, alternative embodiments of the invention may allocate tasks differently.

In an exemplary processing, the downconverted baseband receive samples (RX_IQ) are received by interpolator **300** from the external RF unit of **Fig. 4**. Interpolator **300** generates interpolated samples that are received by searcher subsystem **302** and channel elements **312**. Searcher subsystem **302** performs periodic searching for reverse link signals, and provides the results of those searches to DSP controllers **304** and the external control system (not shown). The external controller (microprocessor) may respond by

determining which signals should be processed, and assigning a channel element **312** for processing the signal. The assignment is typically performed by providing the time offset of the signal to be processed to the particular channel element **312**. In the described embodiment of the invention, each channel element may process multiple multipath instances of a signal, referred to as fingers, where each finger requires a different time offset. Thus, the external controller may provide multiple time offsets to a channel element **312**.

In one embodiment of the invention, the receive samples can be received at one of two rates: twice the spreading chip rate (Chipx2) or eight times the spreading chip rate (Chipx8). When receive samples RX_IQ are received at Chipx2, interpolator **300** interpolates the samples to a rate of eight times the spreading rate (Chipx8). When samples are received at Chipx8, interpolator **300** is bypassed. This allows the system to operate within differently configured system that provide samples at either chipx8 or chipx2.

Digital signal processor (DSP) **304.1** interfaces with channel elements **312.0 - 312.5** and DSP **304.2** interfaces with channel elements **312.6 - 312.11**. Viterbi decoder **316.0** interfaces with deinterleavers **322.0 - 322.3** via medium rate Walsh (W_m) decover 323.0-323.2. Viterbi decoder **316.1** interfaces with deinterleavers **322.4 - 322.7** via medium rate Walsh decover 323.4 - 323.7. Viterbi decoder **316.3** interfaces with deinterleavers **322.8 - 322.11** via medium rate Walsh decover 323.8 -323.11. Channel elements **312** are coupled to deinterleaver- **322** through multiply-accumulate (MAC) **320**. In alternative embodiments of the invention, different numbers of DSPs may be used, including one DSP.

In one embodiment of the invention, channel elements **312** performs various functions including despreading and medium rate Walsh decovering for medium rate transmissions. Additionally, channel element **312** performs symbol dropping on a portion of the data processed for medium rate transmissions. Preferably, the particular amount and portion of data that is dropped depends on the transmission rate of the data being processing and control input from the corresponding DSP **304**.

During an exemplary processing by the demodulator system of **Fig. 4**, DSP **304** receive instructions to process incoming signals that are transmitted at either medium data rates or low data rates and assigns one channel element **312** for processing the signal if it is lower than a particular rate, and assigns two or more channel elements for processing the signal if the signal is transmitted at a data rate above a particular rate. In one embodiment of

the invention, if the signal is transmitted at a low data rate or the medium data rates of rate one or rate two, the microprocessor assigns one channel element **312** to process the signal.

If the signal is transmitted at the medium data rates of rate four or rate eight, DSP **304** assigns more than one channel element **312** to processing the signal. In particular, if the signal is transmitted at the medium data rate of rate four, DSP **304** assigns two channel elements **312** to processing the signal, and if the signal is transmitted at the medium data rate of rate eight, microprocessor assigns four channel elements **312** for processing the signal. Where multiple channel elements are assigned, each channel element processes only a portion of the incoming signals. For example, with two channel elements assigned, each channel element processes one half of the signal. With four channel elements, each channel element processes one fourth of the signal.

Additionally, in one embodiment of the invention DSP **304** or the microprocessor assigns a channel element type (CE_TYPE) to each channel element assigned for processing the higher rate signals (rate four and rate eight in one embodiment of the invention.) The particular portion of the signal processed by a particular channel is determined by the channel element type, one example of which is described in greater detail below.

After a signal is processed by channel elements **312**, the resulting despread chip data is accumulated over a symbol duration by MAC **320**, which preferably performs the accumulation for each channel element in a time-shared manner. Additionally, the MAC calculates the cross product of the pilot traffic channel, and sums the results over the set of fingers being processed by a particular channel element. The resulting accumulated symbol data is forwarded to a deinterleaver **322**, which performs time-shared deinterleaving and demodulation for channel elements. The deinterleaver **322** deinterleaves each 20 ms frame of data received, which for different rate corresponds to different amounts of data. For the higher data rates, the symbol dropping performed by channel elements **312** reduces the amount of data processed by each deinterleaver **322**. This reduces the necessary size of the deinterleaver **322** memory, which substantially reduces the overall circuit area of the demodulator system.

Medium rate Walsh decoverers perform low rate Walsh decovering and forward the decovered soft decision data to Viterbi decoders **316**. For medium rate transmissions, Viterbi decoders **322** decode the soft decision data at the transmission rate specified. For lower rate transmission, Viterbi decoders **316** decode at all the four data rates, with the actual data rate used

determined by error and probability values generated therewith. One method of performing rate determination is described in US Patent 5,566,206 entitled "METHOD AND APPARATUS FOR DETERMINING DATA RATE OF TRANSMITTED VARIABLE RATE DATA IN A COMMUNICATIONS RECEIVER" assigned to the assignee of the present invention and incorporated herein by reference. The output data is then made available for additional processing, which in the exemplary embodiment of the invention involves forwarding to base station controller **14** of **Fig. 1**.

As should be apparent in the described embodiment, a channel element **312**, a deinterleaver **322**, the medium rate Walsh decover **323** and the time-shared MAC **320** form a channel resource. As described throughout the application, the channel resource can be used alone to process some medium and lower rate signals, or in combination with other channel resources to process other medium rate signals (the highest rate medium rate signals).

Fig. 6 is a block diagram of a channel element **312** when configured in accordance with one embodiment of the invention. The RX_IQ samples are received by four finger processors **570**. Each finger processor processes one instance of the particular signal assigned to the associated channel element at a time offset provided from the control system (connection from control system not shown). The resulting demodulated symbols from finger processors **570** are forwarded to MAC **320** of **Fig. 5**.

Fig. 7 is a block diagram of a finger processor **400** when configured in accordance with one embodiment of the invention. Antenna select **500** selects one set of Rx samples from the set of receive samples provided. In accordance with the base station described above, six sets of Rx samples are provided which correspond to two antennas for each sector. The antenna selected is determined by a searcher **306** which searches each incoming set of Rx samples for multipath signals, along with the controller, which generates selection signals provided to antenna select **500**.

The selected Rx samples are forwarded to decimator **502** which decimates the Rx samples down to chipx2. Phase rotator **504** performs an initial phase adjustment of the Rx samples and despreader **505** demodulates the signal using a pseudo noise (PN) spreading code from PN generator **506**. The particular code PN generator **506** generates, and the particular time offset, is determined by timing and control unit **508**, which in turn is controlled by a DSP unit **304.1** based on the search results received by that DSP unit **304.2** from a searcher **306**.

Despreader-decover **505** generates three output sets for the signal being processed by despreading using the PNI and PNQ codes and the control and traffic channel Walsh codes ($W_{C,T}$ and $W_{C,C}$). Each output set is comprised of an in-phase component and a quadrature-phase component. The three output sets correspond to an on time despreading, an early despreading, and a late despreading. The on-time despreading is the best estimate of the time offset of the signal, and in one embodiment of the invention the early despreading is offset _ the duration of a spreading chip before the on-time despreading, and the late despreading is offset _ the duration of a spreading chip after the on-time despreading.

2x accumulator **510** accumulates the despread data over two spreading chips and provides the accumulated on-time data to medium rate repetition decovering circuit **512**. The accumulated early and late despread data is forwarded directly to a DSP **304**. The DSP **304** advances or retards the processing of the signal in response to the early and late despread data via control input to timing and control circuit **507**.

DSP **304** also provides phase rotation information to phase accumulator **511** which provides phase rotation data to rotator **504**.

The on-time accumulated data is received by medium rate repetition decovering circuit **512**. Medium rate repetition decovering circuit **512** accumulates the despread data over a number of symbols that depends on rate at which the data is being transmitted. In particular, the despread data is accumulated over R_M symbols as set forth in Table I depending on the rate at which the data is transmitted. Additionally, if the despread data is being transmitted at a rate two, rate four or rate eight, medium rate repetition decovering circuit **512** decovers the despread data with the corresponding medium rate Walsh code W_M as set forth in Table I. The resulting decovered symbols are forwarded to symbol dropper **516**.

In one embodiment of the invention, symbol dropper **516** drops, or "gates," a portion of the decovered symbols received. In particular, symbol dropper **516** drops a portion of the symbols received for higher data rate transmissions, and passes all the symbols received for lower rate transmissions. The amount of symbols that are dropped by symbols dropper **516** depends on the data rate of the signal being processed. The portion of symbols that are dropped depends on the channel element type CE_TYPE assigned to the channel element **312** in which the finger processor **570** is located.

In the exemplary embodiment of the invention, symbol dropper drops one half (1/2) of the symbols received for rate four transmissions, and

three-fourths (3/4) of the symbols received for rate eight transmissions. That is, one half (1/2) of the symbols are passes for rate four transmissions, and one quarter (1/4) of the symbols are passed for rate eight transmissions.

The particular symbols that are passed and dropped by symbol dropper **516** are determined by the channel element type CE_TYPE assigned to the corresponding channel element **312**. For example, for rate four transmissions, the channel element type CE_TYPE could indicate whether the finger should processes the even or odd symbols. For rate eight transmissions, the channel element type CE_TYPE could indicate which of every four symbols (i.e. the first, second, third or fourth) should be passed.

Thus, to process a rate four or rate eight medium rate signal, a DSP **304** assigns different channel element types CE_TYPE to a set of channel elements **312**, and then assigns that set of channel elements to process the same medium rate signal. The result is that each channel element **312** processes a different portion of the same signal, and the set of channel elements **312** together process the entire signal. The resulting different portions of the data can be combined later in the processing yielding the entire signal.

As described in greater detail below, by dropping a portion of the signal before that signal is deinterleaved, the size of the deinterleaver for each channel element can be reduced. The deinterleaver typically requires substantial amounts of memory, and memory takes up significant amounts of circuit area on the integrated circuit. Thus, the circuit area necessary to implement the integrated circuit is reduced.

The despread symbols are forwarded to data buffer **514**. Data buffer **514** stores 128 eight (8) bit symbol values for the in-phase and quadrature phase portions of the signal being processed. The despread symbols are delayed within data buffer **514** to eliminate the time skew between the various fingers of the signal being processed within the channel element. MAC unit **402** receives the deskewed symbols and sums the data from the four fingers generating combined despread symbols.

Fig. 8 is a block diagram of deinterleaver **322** (**Fig. 5**) and a medium rate Walsh code decover **323** when configured in accordance with one embodiment of the invention. Combined despread symbols are received by deinterleaver RAM **600**. In one embodiment of the invention deinterleaver RAM is 1536x4 bits, which is sufficient to store 1536 four bit symbols. 1536 symbols represents one fourth of the symbols received in a 20 ms frame transmitted at rate eight, or one half the symbols received in a 20 ms frame

transmitted at rate four. Additionally, 1536 symbols represents the total number of symbols in a 20 ms frames for rate two or below, given the medium rate symbol repetition R_M. In another embodiment of the invention, the interleaver is 1536x8 to allow double buffering.

Under the control of deinterleaver address control **601**, the symbols stored in deinterleaver are read out in deinterleaved fashion to XOR gates **602**. XOR gates **602** decover the symbols with the four lower rate Walsh codes ($W_{1/8}$, $W_{1/4}$, $W_{1/2}$ and W_{FULL}). The resulting decovered symbols are accumulated by accumulators **604** over the number of Walsh chips in the corresponding low rate Walsh codes. The decovered symbols, along with an additional copy of the deinterleaved symbols are forwarded to the corresponding Viterbi decoder **316**. In another embodiment of the invention a single XOR gate and accumulator are used in a time-shared fashion. For lower rate transmissions, the Viterbi decoder **316** decodes at all four data rates and determines the correct data rate based on any errors detected during the decoding.

Modulation with the low rate Walsh codes facilitates the determination of the rate that is transmitted, because different rates are modulated with codes that are orthogonal to one another. Thus, decovering with a low rate Walsh code does not correspond to the actual transmission rate of the frame should yield a low energy value compared to the energy level of the corrected decovered symbols.

For medium rate transmissions, the uncovered symbols are decoded by the Viterbi decoder **316** at the corresponding data rate as configured by the microprocessor.

Fig. 9 (2-13) is a block diagram of repetition decovering and symbol drop circuit **516** when configured in accordance with one embodiment of the invention. The data being processed is received within latches **710** (multi-bit latches) on in-phase input DATA_I and quadrature phase input DATA_Q. The outputs of latches **710** are applied to the B inputs of adder/subtractors **705**, and also form the outputs of the medium rate repetition decovering circuit **512**. The A inputs of adder/subtractors **705** receive the on time despread chip data from 2x accumulator **510**. Adder/subtractors **705** add or subtract the inputs A and B based on the signal applied to control the input +/-.

Walsh code generator **700**, generates the medium rate Walsh code W_M in accordance with the transmission rate of the data being processed. The resulting Walsh code is applied to the control input of adder/subtractors **705** specifying whether an add or subtract operation should be performed.

Together adder/subtractors **705** and latches **710** act as an accumulator where the input is either added or subtracted from the accumulated value based on the logic level of the medium rate Walsh code W_M. The effect is that the despread data is demodulated by the medium rate Walsh code, and the resulting demodulated data is accumulated over the length of the medium rate Walsh code. Accumulator clear generator **712** resets the value of latches **710** each medium rate repeat value R_M the for the repeat value R_M. The resulting medium rate decovered symbols are forwarded to symbol dropper **516**. Various alternative methods for performing applying the Walsh code should be apparent.

Fig. 10 is a block diagram of the symbol drop block when configured in accordance with one embodiment of the invention. The decovered symbols (DSYMBOL_I & DSYMBOL_Q) are received by latches **810** from medium rate repetition decovering circuit **512**. Symbol select enable generator **800** receives the channel element type CE_TYPE and generates a symbol enable signal that is applied to the enable inputs of latches **810**.

Symbol select enable generator **800** provides an exemplary circuit and method for generating the symbol enable signal based on the channel element type CE_TYPE. A two bit counter value which increments with each new symbol (CNT(0:1)) is applied to one input of comparators **802**. AND gates may also be used in place of comparators. The other input of comparators **802** receives a hardwired binary number as shown. The outputs of comparators **802** are applied to multiplexer **804**, which is controlled by CE_TYPE. The output of multiplexer **804** is received by one input of OR gate **805**, while the other input of OR gate **805** receives a logic high when CE_TYPE = 6 or 7.

In one embodiment of the invention, the channel element type CE_TYPE can be any value from 0 to 7. Values 0 - 3 correspond to channel element types that are used for rate eight transmissions. Values 4 and 5 correspond to channel element types that are used for rate four transmissions. Values 6 and 7 correspond to channel element types that are used for rate two or below transmissions.

As described above, four channel elements are used to process a signal transmitted at rate eight. For the four CE_TYPEs 0 - 3, the symbol enable signal is asserted once every four symbol times, where the particular symbol time at which the signal is asserted is different for each CE_TYPE 0 -3. For example, for CE_TYPE 0, the symbol enable signal is asserted during the first of every four symbol times. For CE_TYPE 1, the symbol enable signal is asserted during the second of every four symbol times.

Similarly, for the two CE_TYPEs 4 and 5, the symbol enable signal is asserted once every other symbol time, where the particular symbol time is different for each CE_TYPE. For CE_TYPEs 6 and 7, the symbol enable signal is asserted each symbol time.

Thus, to processes a signal transmitted at a higher transmission rate, a microprocessor assigns a set of channel elements to processes the signal, and then assigns each channel element a different channel element type CE_TYPE. Each channel element responds by processing a different portion of the signal, with the sum of all the portions of the signal processed equaling the entire signal.

By having each channel element process only a portion of the signal, the capability of each channel element, and each channel element resource, is reduced. This reduces the total circuit area of the integrated circuit used to implement the demodulator, and therefore increases efficiency and reduces cost. In contrast, a system that configures each channel resource with the ability to process the high rate transmission will have resources go unused during lower rate transmissions. By providing channel resources that can operate together on the same transmission, overall usage and efficiency is increased.

Also, since in many CDMA systems the total communications capability is limited, when the number of higher rate communications conducted is increased, the number of lower rate communications conducted is reduced. Thus, by having a demodulation system where a number of lower rate demodulation resources can be combined to demodulate a higher rate transmission, the capacity and allocation of demodulation resources more closely matches the transmission capability of the CDMA system. Matching resources with capability further increases efficiency.

WE CLAIM:

CLAIMS

1. A demodulator for demodulating a higher rate signal and a lower rate signal comprising:

first channel resource for demodulating substantially all of said lower rate signal and for demodulating a first portion of said higher rate signal;

second channel resource for demodulating a second portion of said higher rate signal, wherein said first portion is substantially different from said second portion.

2. The demodulator of claim 1 wherein said first channel resource is comprised of a first symbol dropper for selecting said first portion of said higher rate signal.

3. The demodulator of claim 2 wherein said second channel resource is comprised of a second symbol dropper for selecting said second portion of said higher rate signal.

4. The demodulator of claim 2 further comprising first deinterleaver memory having a size sufficient to store a full frame of said lower rate signal, and said first portion of said higher rate signal.

5. The demodulator of claim 4 further comprising second deinterleaver memory having a size sufficient to store said second portion of said higher rate frame.

6. The demodulator of claim 5 wherein said second deinterleaver memory also has a size sufficient to store a full frame of said lower rate signal.

7. The demodulator of claim 1 wherein said first portion and said second portion have substantially the same format.

8. The demodulator of claim 7 wherein said first portion contains first user data and first control data in a first order and said second portion contains second user data and second control data in a second order, wherein said first order and said second order are substantially the same.

9. The demodulator of claim 8 wherein said first user data has a format substantially similar to said first portion and said second portion.

10. A demodulator comprising:
first circuit for demodulating a first portion of a lower rate signal and a second portion of a higher rate signal; and
second circuit for demodulating a third portion of said higher rate signal, wherein said first portion is larger than said second portion and said third portion, and
said second portion and said third portion are substantially different.

11. The demodulator of claim 10 wherein said first portion is all of said lower rate signal, and said second portion is part of said higher rate signal.

12. A method for demodulating a higher rate signal and a lower rate signal comprising the steps of:
a) demodulating substantially all of said lower rate signal;
b) demodulating a first portion of said higher rate signal;
c) demodulating a second portion of said higher rate signal, wherein said first portion is substantially different from said second portion.

13. The method of claim 12 wherein step b) is comprised of the step of dropping said second portion of said higher rate signal.

14. The method of claim 13 wherein step c) is comprised of the step of dropping said first portion of said higher rate signal.

15. The method of claim 13 further comprising the steps of:
storing a full frame of said lower rate signal;
deinterleaving said full frame of said lower rate signal;
storing said first portion of said higher rate signal; and
deinterleaving said first portion of said higher rate signal.

16. The method of claim 15 further comprising the steps of:
storing said second portion of said higher rate signal; and
deinterleaving said second portion of said higher rate signal.

17. The method of claim 12 wherein said first portion and said second portion have substantially the same data format.

18. The method of claim 17 wherein said first portion contains first user data and first control data in a first order and said second portion contains second user data and second control data in a second order, wherein said first order and said second order are substantially the same.

19. The method of claim 18 wherein said first portion has a format substantially similar to said first portion and said second portion.

20. A receive processing system comprising:

a first receive processing system for processing one lower rate signal in a first mode and for processing a first portion of a higher rate signal in a second mode;

a second receive processing system for processing one lower rate signal in said first mode and for processing a second portion of said higher rate signal is a second mode.

21. The receive system of claim 20 wherein said first receive processing system is comprised of a first symbol dropper for selecting said first portion of said higher rate signal.

22. The receive system of claim 21 wherein said second receive processing system is comprised of a second symbol dropper for selecting said second portion of said higher rate signal.

23. The receive system of claim 21 wherein said first receive processing system is comprised of: a first deinterleaver memory having a size that is less than that necessary to store said first portion of said higher rate signal and said second portion of said higher rate signal.

24. The receive system of claim 23 wherein said second receive processing system is comprised of: a second deinterleaver memory having a size that is less than that necessary to store said first portion of said higher rate signal and said second portion of said higher rate signal.

25. The receive system of claim 21 wherein said second deinterleaver memory has a size sufficient to store a full frame of said lower rate signal.

26. The receive system of claim 21 wherein said first portion and said second portion have substantially the same format.

27. The receive system of claim 21 wherein said first portion contains first user data and first control data in a first order and said second portion contains second user data and second control data in a second order, wherein said first order and said second order are substantially the same.

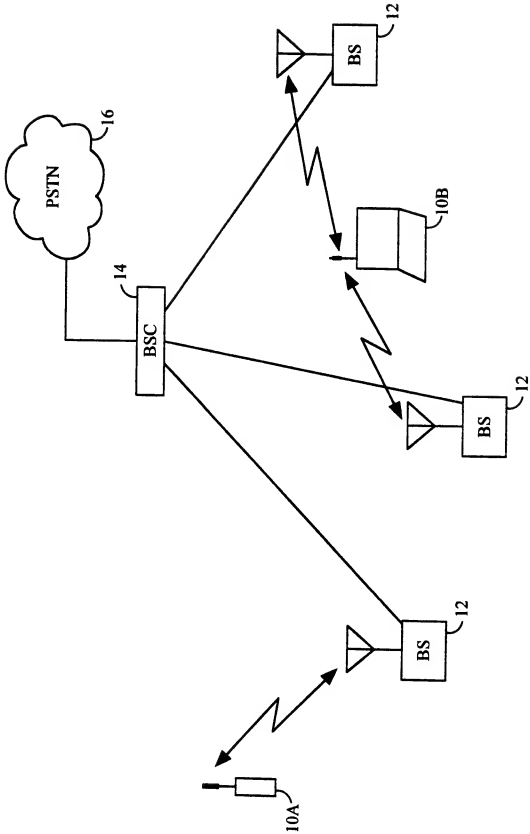

FIG. 1

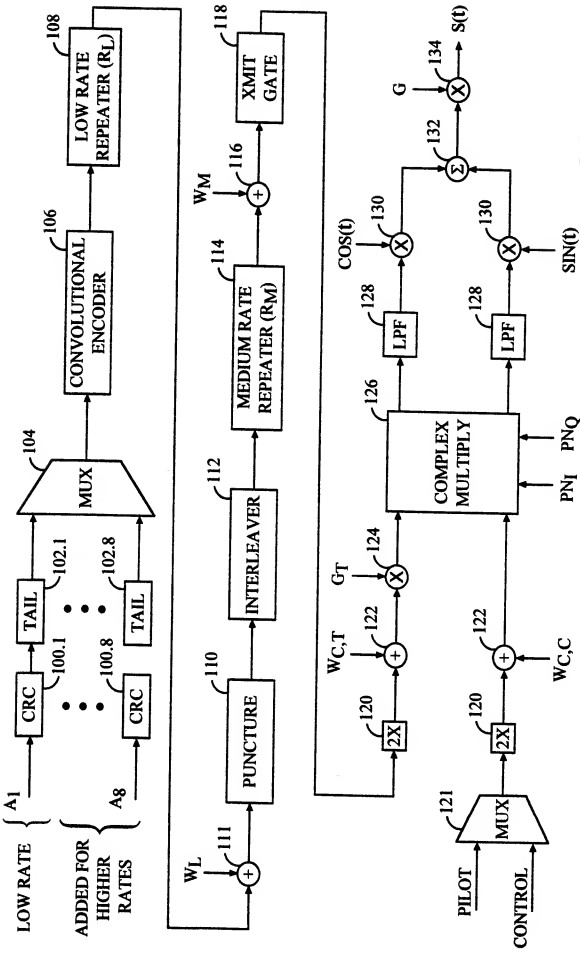
LOW RATE
ADDED FOR HIGHER RATES
A1
A8
CRC
CRC
TAIL
TAIL
100.1
100.8
102.1
102.8
MUX
104
CONVOLUTIONAL ENCODER
106
LOW RATE REPEATER (RL)
108
PUNCTURE
110
INTERLEAVER
112
MEDIUM RATE REPEATER (RM)
114
XMIT GATE
118
WL
111
WM
116
WC,T
122
GT
124
120
2X
COMPLEX MULTIPLY
126
LPF
128
COS(t)
130
SIN(t)
130
Σ
132
G
134
S(t)
PNI
PNQ
PILOT
CONTROL
MUX
121
WC,C
122
120
2X

FIG. 2

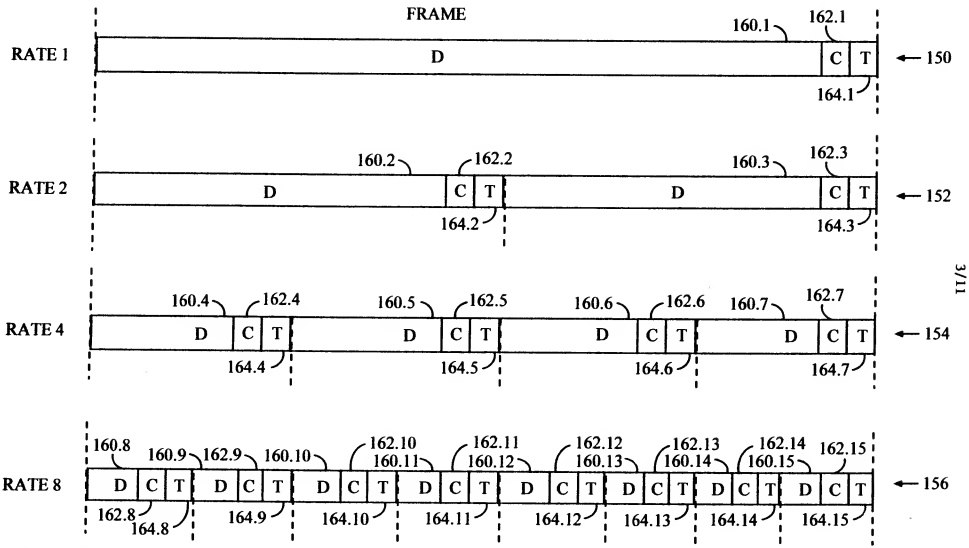
FRAME
RATE 1
D
C
T
160.1
162.1
164.1
150
RATE 2
160.2
162.2
164.2
160.3
162.3
164.3
152
RATE 4
160.4
162.4
164.4
160.5
162.5
164.5
160.6
162.6
164.6
160.7
162.7
164.7
154
RATE 8
160.8
160.9
160.10
160.11
162.8
164.8
162.9
164.9
162.10
164.10
162.11
160.12
164.11
162.12
160.13
164.12
162.13
160.14
164.13
162.14
160.15
164.14
162.15
164.15
156
D = DATA
C = CRC
T = TAIL

FIG. 3A

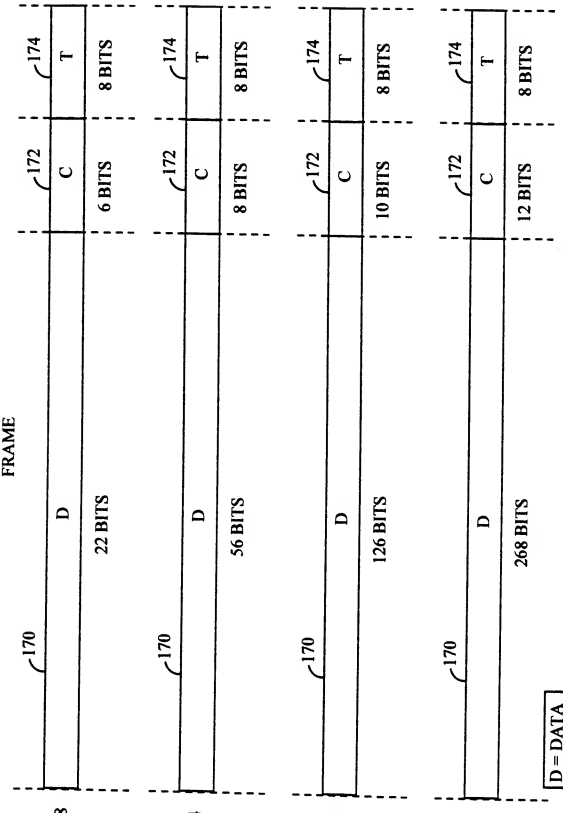
FRAME
170
172
174
RATE 1/8
D
C
T
22 BITS
6 BITS
8 BITS
RATE 1/4
56 BITS
8 BITS
8 BITS
RATE 1/2
126 BITS
10 BITS
8 BITS
RATE 1
268 BITS
12 BITS
8 BITS
D = DATA
C = CRC
T = TAIL

FIG. 3B

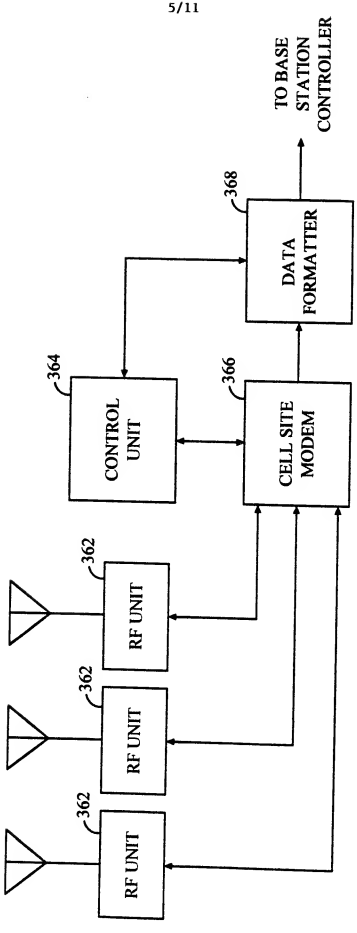
TO BASE STATION CONTROLLER
368
DATA FORMATTER
364
CONTROL UNIT
366
CELL SITE MODEM
362
RF UNIT
362
RF UNIT
362
RF UNIT
BASE STATION

FIG. 4

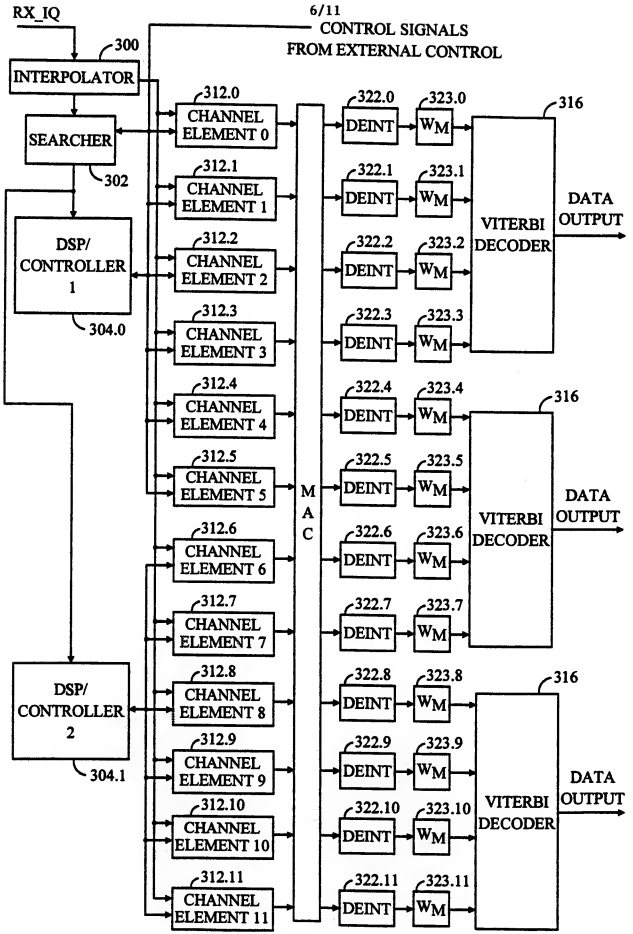
RX_IQ
CONTROL SIGNALS
FROM EXTERNAL CONTROL
300
INTERPOLATOR
SEARCHER
302
DSP/
CONTROLLER
1
304.0
DSP/
CONTROLLER
2
304.1
312.0
CHANNEL
ELEMENT 0
312.1
CHANNEL
ELEMENT 1
312.2
CHANNEL
ELEMENT 2
312.3
CHANNEL
ELEMENT 3
312.4
CHANNEL
ELEMENT 4
312.5
CHANNEL
ELEMENT 5
312.6
CHANNEL
ELEMENT 6
312.7
CHANNEL
ELEMENT 7
312.8
CHANNEL
ELEMENT 8
312.9
CHANNEL
ELEMENT 9
312.10
CHANNEL
ELEMENT 10
312.11
CHANNEL
ELEMENT 11
MAC
322.0
DEINT
323.0
WM
322.1
DEINT
323.1
WM
322.2
DEINT
323.2
WM
322.3
DEINT
323.3
WM
322.4
DEINT
323.4
WM
322.5
DEINT
323.5
WM
322.6
DEINT
323.6
WM
322.7
DEINT
323.7
WM
322.8
DEINT
323.8
WM
322.9
DEINT
323.9
WM
322.10
DEINT
323.10
WM
322.11
DEINT
323.11
WM
316
VITERBI
DECODER
DATA
OUTPUT
316
VITERBI
DECODER
DATA
OUTPUT
316
VITERBI
DECODER
DATA
OUTPUT

FIG. 5

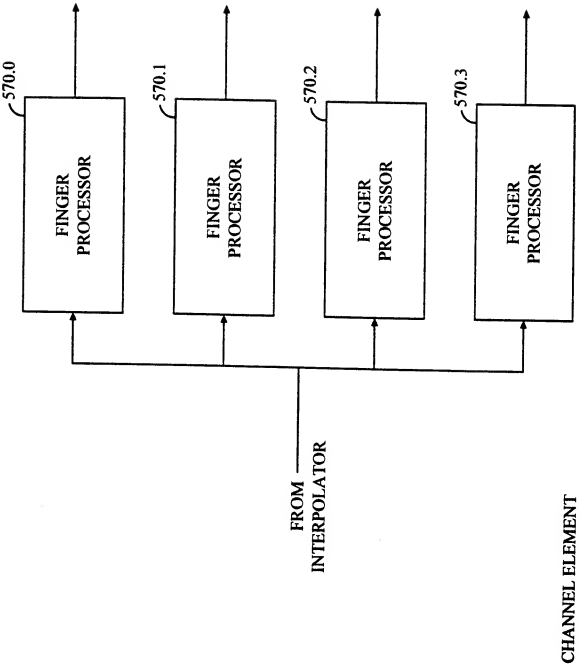
CHANNEL ELEMENT
FROM INTERPOLATOR
570.0
FINGER PROCESSOR
570.1
FINGER PROCESSOR
570.2
FINGER PROCESSOR
570.3
FINGER PROCESSOR
TO MAC

FIG. 6

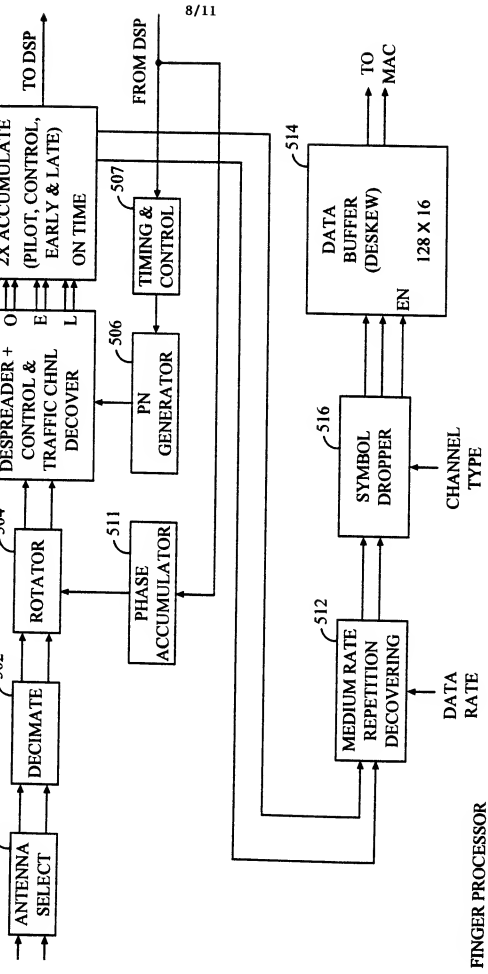
FINGER PROCESSOR
500
ANTENNA SELECT
502
DECIMATE
504
ROTATOR
505
DESPREADER + CONTROL & TRAFFIC CHNL DECOVER
O
E
L
506
PN GENERATOR
507
TIMING & CONTROL
510
2X ACCUMULATE (PILOT, CONTROL, EARLY & LATE) ON TIME
TO DSP
FROM DSP
511
PHASE ACCUMULATOR
512
MEDIUM RATE REPETITION DECOVERING
DATA RATE
514
DATA BUFFER (DESKEW)
128 X 16
EN
TO MAC
516
SYMBOL DROPPER
CHANNEL TYPE

FIG. 7

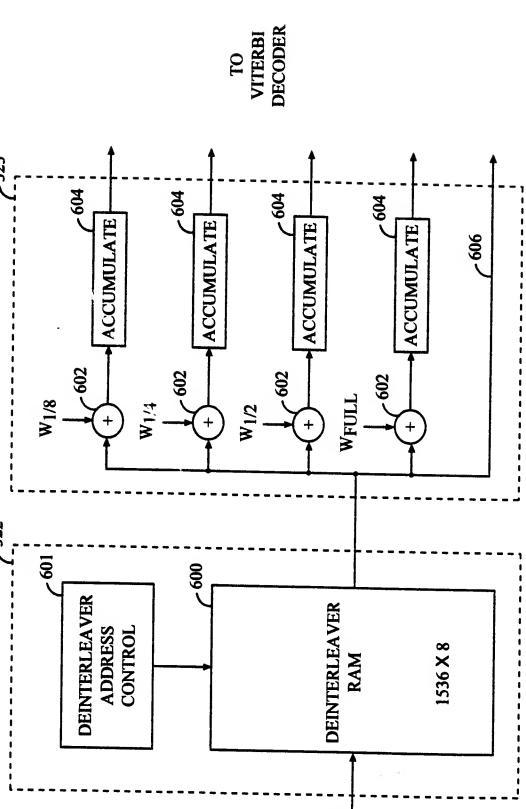
322
601
DEINTERLEAVER ADDRESS CONTROL
600
DEINTERLEAVER RAM
1536 X 8
FROM MAC
COMBINED_ DROP_DATA
323
W1/8
W1/4
W1/2
WFULL
602
604
ACCUMULATE
606
TO VITERBI DECODER
DEINTERLEAVER/LOW RATE DEMODULATOR

FIG. 8

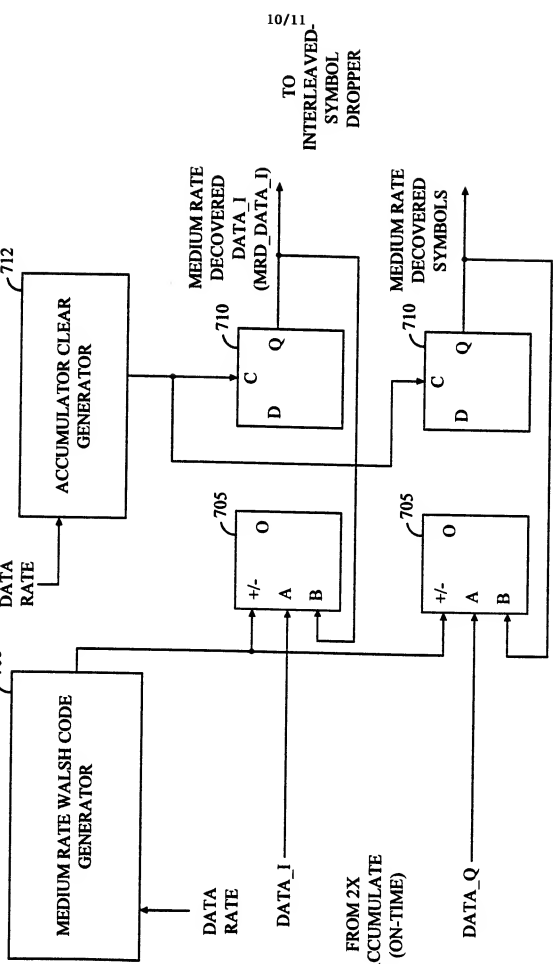
MEDIUM RATE WALSH CODE GENERATOR
700
DATA RATE
DATA_I
FROM 2X ACCUMULATE (ON-TIME)
DATA_Q
MEDIUM RATE REPETITION DECOVERING
DATA RATE
ACCUMULATOR CLEAR GENERATOR
712
705
+/-
A
B
O
705
+/-
A
B
O
710
D
C
Q
MEDIUM RATE DECOVERED DATA_I (MRD_DATA_I)
710
D
C
Q
MEDIUM RATE DECOVERED SYMBOLS
TO INTERLEAVED-SYMBOL DROPPER

FIG. 9

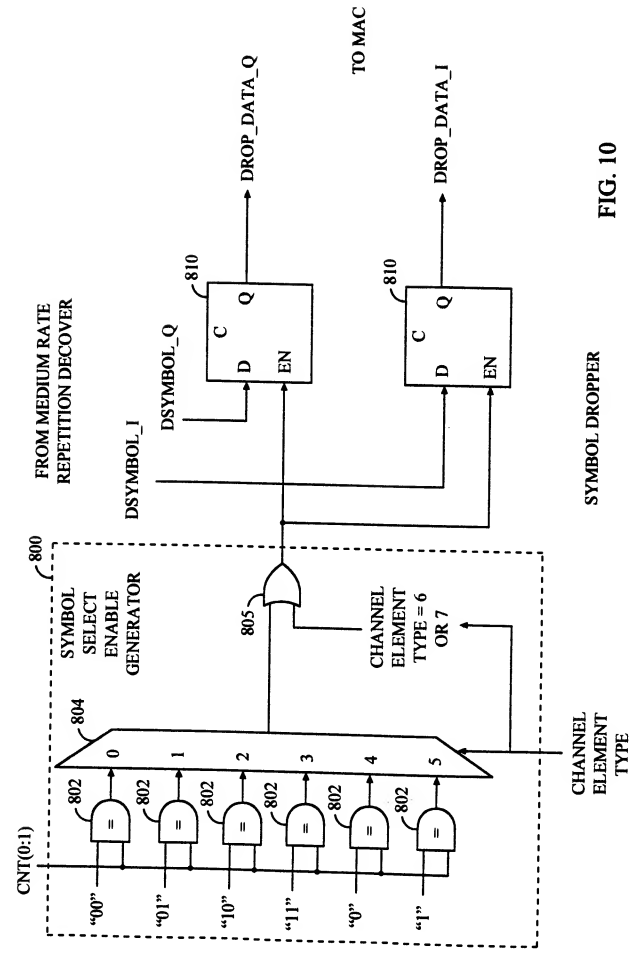
CNT(0:1)
"00"
"01"
"10"
"11"
"0"
"1"
802
=
804
0
1
2
3
4
5
CHANNEL ELEMENT TYPE
800
SYMBOL SELECT ENABLE GENERATOR
805
CHANNEL ELEMENT TYPE = 6 OR 7
FROM MEDIUM RATE REPETITION DECOVER
DSYMBOL_I
DSYMBOL_Q
810
C
D
Q
EN
DROP_DATA_Q
DROP_DATA_I
TO MAC
SYMBOL DROPPER

FIG. 10

INTERNATIONAL SEARCH REPORT

Int tional Application No
PCT/US 99/27593

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04B1/707

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04B H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 828 361 A (NOKIA MOBILE PHONES LTD) 11 March 1998 (1998-03-11) column 2, line 12 -column 3, line 44 column 5, line 5 -column 6, line 11; figure 1A column 10, line 12 -column 11, line 11; figure 1B	1,7,10, 12,19, 20,26
A	EP 0 809 364 A (MITSUBISHI ELECTRIC CORP) 26 November 1997 (1997-11-26) page 10, line 36 - line 56; figures 1-3	1,10,12, 20

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
12 May 2000	18/05/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Bossen, M

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Int ational Application No
PCT/US 99/27593

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0828361 A	11-03-1998	NONE	
EP 0809364 A	26-11-1997	JP 9312629 A	02-12-1997
		AU 711686 B	21-10-1999
		AU 7649396 A	27-11-1997
		CA 2194722 A	21-11-1997
		CN 1166094 A	26-11-1997
		NO 970010 A	21-11-1997
		US 5966377 A	12-10-1999